Low Power and High Linear, 28 GHz Low Noise Amplifier Designed in 22nm FDSOI Technology

Marzieh Mollaalipouramir, Herbert Zirath, Christian Fager
Chalmers University of Technology, Gothenburg, Sweden

Summary

This abstract presents a high-performance and low-power LNA design using 22nm FDSOI process. The LNA utilizes a common source topology that is inductively degenerated includes a cascode device.
Operating at a frequency of 28GHz, the LNA produces a gain of 11dB, with an input-referred third-order intercept point (IIP3) of 2.0dBm. The LNA's 3-dB bandwidth is 14GHz. The LNA's minimum noise figure (NF) is 2dB at 30GHz, while the power dissipation (PDC) is 6.3mW.

1. Introduction

With the rapid increase of portable wireless devices and wireless networks, the need for low-power and High linear RF front-end circuits has been growing.
As the first active block in the RF front-end of a receiver, the LNA needs to provide, low noise, high gain, modest linearity, and low power consumption.
As the initial active component in a receiver's RF front-end, the low-noise amplifier (LNA) must deliver multiple functions simultaneously, such as broad frequency range, low noise, high amplification, and reasonable linearity, which all necessitate the utilization of high power consumption. In this work a low-power cacode LNA has been designed. By applying a small inductor to the gate of the cascode transistor the linearity and stability has been improved.

2. Design Process and Results

Figure 1 shows a schematic view of the LNA based on inductively degenerated common source topology with a cascade device. The gate of M2 is retained at a fixed DC voltage, to keep both transistors in saturation all the time. An inductive load is used to save overhead voltage while enhancing the LNA voltage gain.
To achieve simultaneous noise and impedance matching, a source degeneration inductor Ls is added. This technique can make the minimum noise figure point (Γopt) and input conjugate point (ΓMS) point close to each other on the Smith chart.
In order to find the optimal bias and sizes for designing a low-power and high-linear circuit, several parameter sweeps simulation has been done
The supply voltage (Vdd) is set as 1V, since there are two transistors (CS and CG) that need to be biased.
According to these figures for larger widths, the power consumption will be higher but gm and gm/gds are also higher leading to higher gain.
The total device width of M1 and M2 were determined based on trade-offs among noise and power dissipation (ID) and gain. To minimize the power consumption and achieve an optimum Nfmin and high gain, the size of M1 was chosen to be 50 µm.
For the selected width, NFmin= 1.32dB , IDD= 5.92mA , gm/gds=36
The decoupling capacitor for the cascode device gate (CG) was carefully designed to ensure circuit stability without a series resistor at the output. The capacitor for the cascode device gate (CG) was reduced to 17 fF. By selecting a small capacitor the circuit is a combination of cascade and cascade structure. The simulation results show the circuit is more linear and stable by selecting a smaller capacitor. But the gain is also decreased.

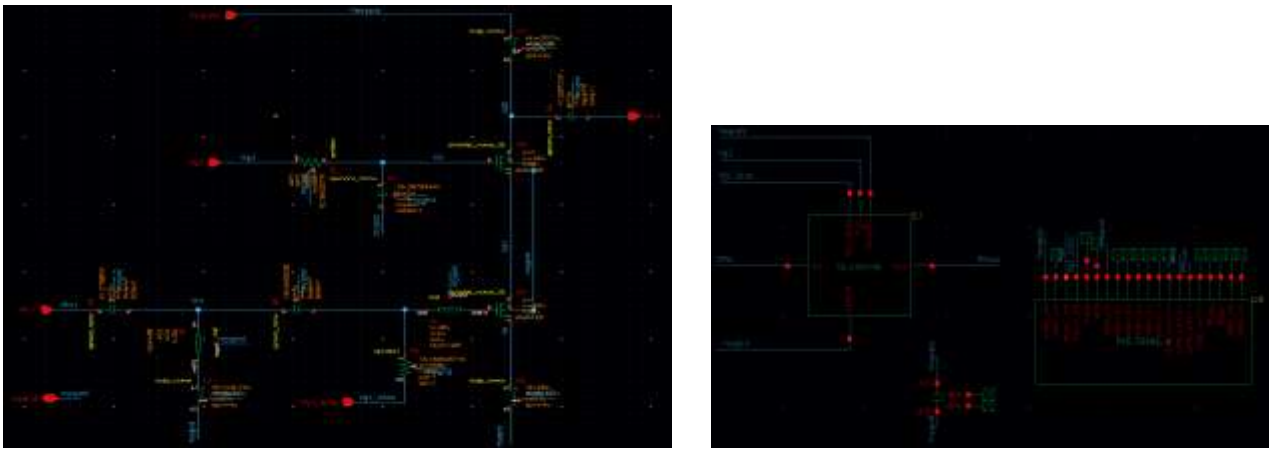


Figure 1. Schematic view of the LNA

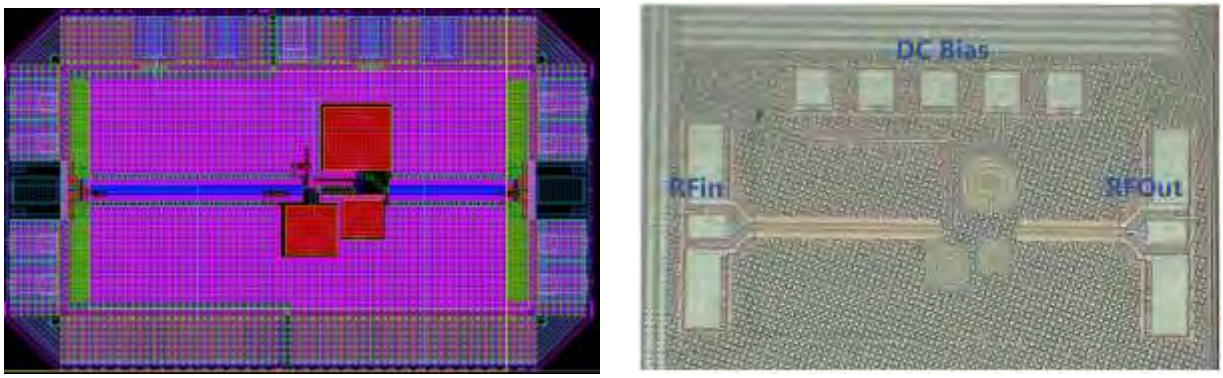
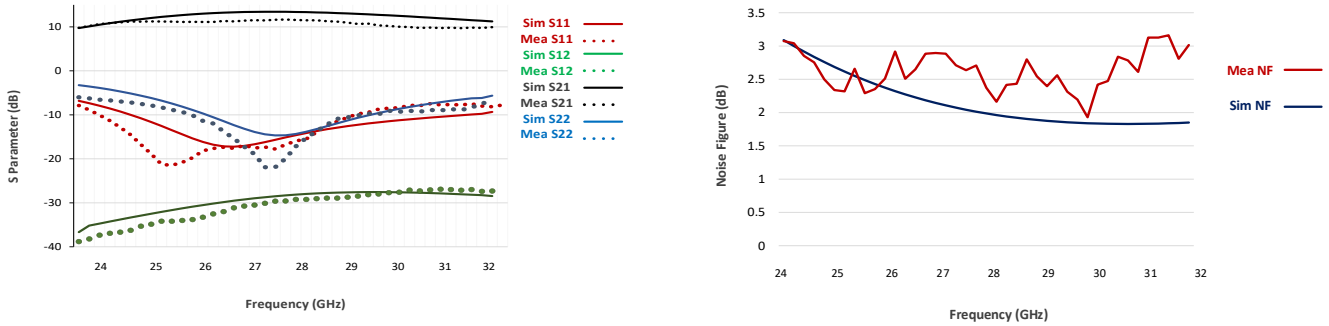


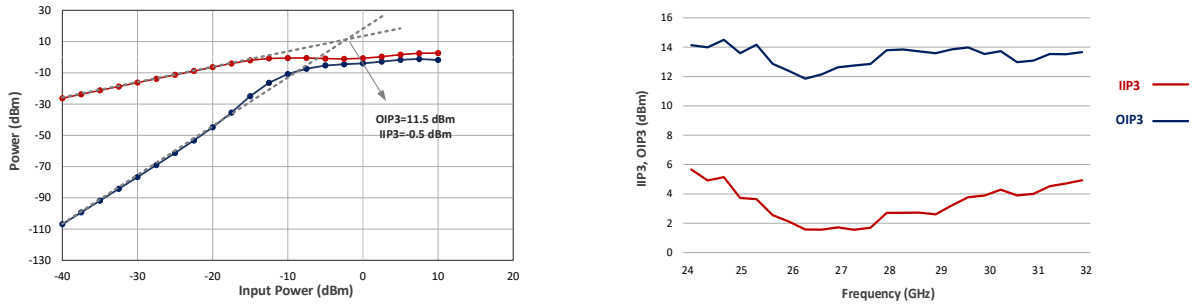
Figure 2. Layout and Chip photograph of the fabricated LNA.

Figure 2 shows the layout and the micrograph of the LNA prototype fabricated in GlobalFoundries, 22-nm FD-SOI CMOS technology (22FDX). The area of the chip is 520 x 810 um2 including bonding pads. Less than 30%, 200 x 220 um2 of the chip area is used for the active devices.



(a) **(b)**

Figure 3. a) Simulated and Measured SP b) Simulated and Measured NF, versus RF input frequency



(a) **(b)**

Figure 4.a) Simulated IIP3, OIP3 versus input power b) Musured IIP3, OIP3 versus input power

Figure 3 and Figure 4 show the measurement result for SP and noise for the LNA which have good agreement with the simulation result. S21 and Noise are around 2dB and 1dB higher than the simulation respectively. IIP3 and OIP3 have been measured and simulated as shown in figure 4 for 20 MHz offset frequency. The measured results are around 1dB higher than the simulation.

References

[1] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin and K. Entesari, "A wideband variable gain LNA with high OIP3 for 5G using 40-nm bulk CMOS", IEEE Microw. Wireless Compon. Lett., vol. 28, no. 1, pp. 64-66, Jan. 2018.
[2] M. K. Hedayati, A. Abdipour, R. S. Shirazi, C. Cetintepe and R. B. Staszewski, "A 33-GHz LNA for 5G wireless systems in 28-nm bulk CMOS", IEEE Trans. Circuits Syst. II Exp. Briefs, vol. 65, no. 10, pp. 1460-1464, Oct. 2018.
[3] C. Li, O. El-Aassar, A. Kumar, M. Boenke, and G. M. Rebeiz, “LNA Design with CMOS SOI Process-l.4dB NF K/Ka band LNA,” in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2018, pp. 1484–1486.
[4] O. El-Aassar, And G. M. Rebeiz, "Design Of Low-Power Sub-2.4 Db Mean NF 5G Lnas Using Forward Body Bias In 22 Nm FDSOI "IEEE Transactions On Microwave Theory And Techniques, vol. 68, no. 10, October 2020.
[5] Bolun Cui, And John R. Long "A 1.7-Db Minimum NF, 22–32-Ghz Low-Noise Feedback Amplifier With Multistage Noise Matching In 22-Nm FD-SOI CMOS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 55, NO. 5, MAY 2020.